Abstract of the Disclosure

A semiconductor memory device and a method of making and using a semiconductor memory device containing a word line design, which is used in ultra-large scale integrated (ULSI) circuits, that produces a device with a lower RC time constant than devices formed using prior art techniques. In one embodiment of the invention low resistivity metal strapping layers are attached to alternating halves of wordlines in a single memory array. The alternating pattern allows the low resistivity of the strapping layers to be utilized without introducing significant negative capacitive resistance effects due to strapping layers being too close to each other.